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A new method to fabricate thin oxynitride/oxide gate dielectric for deep submicron devices

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In this paper, we report a new method to fabricate oxynitride/oxide gate dielectrics for MOS devices. This method utilizes a thin layer of oxynitride as a membrane for controlled diffusion of O_2 and oxidation of Si at high temperatures with low thermal budget. MOS devices made with these oxynitride/oxide structures have interface properties like thermal SiO_2 with a structure resistant to boron diffusion.

1. INTRODUCTION

Deep submicron devices with 0.1 -0.25 μm gate dimensions require ultra thin gate oxides, 40-60 Å equivalent of SiO_2 thickness. Thermal SiO_2 in this thickness range has four major problems:
1. Oxides in this thickness range have large pin-hole density[1].
2. It is difficult to control thickness uniformity of thin oxides by oxidation at high temperatures.
3. Oxidation of silicon at temperatures less than 900 °C generates large compressive stress and high fixed charge [2].
4. For ultrathin oxides, dopants from the p+ poly gate can easily diffuse into the device channel[3]

Various types of oxynitride processes ROXNOX or N_2O etc. have been reported to retard the boron penetration[4-6]. ROXNOX degrade the channel mobility and have high fixed charge. Both ROXNOX and N_2O need high temperature to incorporate few percent N into the oxynitride. We report a new method to fabricate ultra thin oxynitride/oxide(OXN/OX) structures which can be fabricated with low thermal budget.

2. APPROACH

As shown in figure 1, this new approach involves the slow diffusion of O_2 through a thin oxynitride(40-50Å) layer with N/O ratio less than 0.4. This slow diffusion of O_2 through the oxynitride can be utilized to do a controlled 10-15 Å oxide growth at relatively high temperatures ≥ 950 °C. The 10-15Å of silicon dioxide grown at high temperature, but at a slow rate, controls the interface properties and the top oxynitride layer acts as a barrier for boron diffusion.

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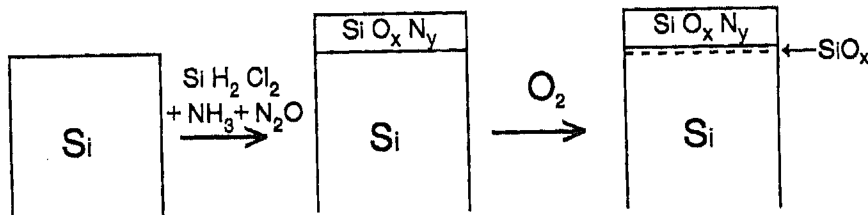


Figure 1: Schematic diagram of the OXN/OX process.

3. FABRICATION

This dual layer of oxynitride/oxide was fabricated by the following method. A thin layer(~50Å) of oxynitride was deposited on <100> P or N Si. The oxynitride chemistry was controlled by the ratio of SiH_2Cl_2, NH_3 and N_2O and deposition temperature. The N/O ratio of the film was varied by changing the ratio of NH_3/N_2O. The N/O ratio was selected to give a desired rate of oxide growth. The deposition rate was ~1Å/min. Figure 2 compares the rate of oxidation through a pure silicon dioxide and through an oxynitride layer with N/O ratio of 0.2. This slow oxidation results in a thin 10-15Å layer of silicon dioxide near the silicon interface. Figure 3 shows a high resolution de-focussed image of the oxynitride/oxide structure. The image clearly shows the presence of a second layer near the silicon interface. (Except for the TEM data, the thickness t_{ox} for the OXN and the OXN/OX structures is equivalent thickness of SiO_2).

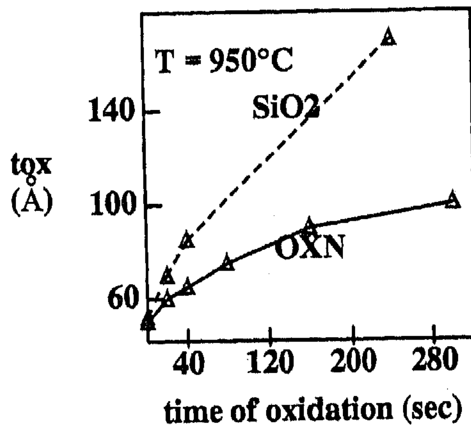
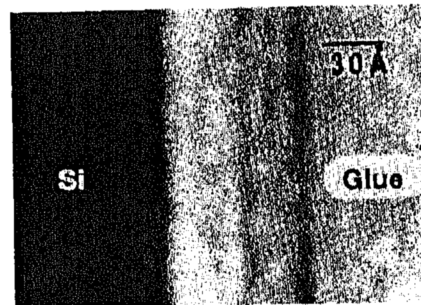


Figure 2: Oxidation through 50Å OXN and 52Å oxide.



Dual Layer

Figure 3: HRTEM(de-focussed) image of OXN/OX structure.

4. ELECTRICAL CHARACTERISTICS

Electrical characteristics of these dual layer OXN/OX structures were evaluated on MOS capacitors with Al or n+ poly gate or MOS transistors with p+ poly gate. As expected, MOS capacitors with the OXN do not have very good dielectric/Si interface. The interface properties start improving after oxidation. For the OXN structures, the fixed charge density Q_f varied from $-3x10^{11}/cm^2$ to $3x10^{11}/cm^2$. For the corresponding OXN/OX structures, oxidized at 950°C for 40 sec-80sec, the Q_f varies from $5x10^{10}/cm^2$ to $7x10^{11}/cm^2$. This fixed charge in OXN/OX structure was reduced to 1-3x10^{11} by the high temperature argon anneal for 40 sec at 950°C. These data imply that OXN structures may have tensile stress and the OXN/OX structure may have compressive stress at the silicon interface.
The change in the nature of the interface can also be seen in the I-V characteristics(Fig.4) for OXN and OXN/OX MOS capacitors. At the same electric field, the leakage current density for the OXN/OX capacitors is much lower than the OXN capacitors. Figure 5 shows the C-V characteristics of OXN/OX structure with poly gate. These samples were oxidized for 40 sec at 950 °C and argon annealed at the same temperature and for the same time. As seen in this figure the OXN/OX/Si structure has a good interface and the interface state density of $<5x10^{10}/cm^2$ at the OX/Si interface.

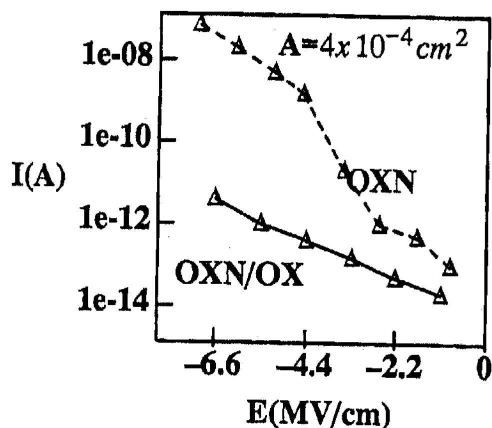


Figure 4: I-V characteristics of OXN and OXN/OX structures.

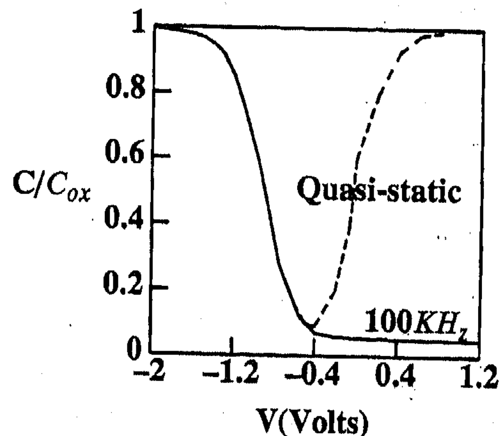


Figure 5: High and low frequency C-V curves of OXN/OX structure.

Boron penetration studies were also done with p+poly/OXN/OX/Si structures. Transistors subjected to 800 °C, 60min plus 850 °C, 60min show the same threshold voltage as the transistors subjected to only 800 °C, 60 min. These data imply the OXN/OX gate dielectric retard boron penetration.

The table summarizes the electrical data on MOS capacitors and p-channel transistors with OXN/OX and SiO_2 of the same thickness. These data clearly show that OXN/OX and pure silicon dioxide of the same thickness have similar electrical characteristics.

Table: Summary of Electrical Results

Parameter	OXN(46Å)	OXN/OX(63Å)	SiO_2(60Å)
Q_f/cm^2	-3–+3x10^{11}	0.5–7x10^{11}	
Q_f/cm^2 with Ar An.		1–3x10^{11}	1.5x10^{11}
Av. Current/cm^2(at 3MV/cm)	2x10^{-8}A	5x10^{-10}A	5x10^{-10}A
Mobility for Holes(cm^2/V-s)	-	110	116
ΔV_t due to B		0	Varies with process

5. SUMMARY

Oxynitride/oxide structures show that oxidation kinetics can be controlled by a diffusion barrier such as oxynitride. The interface charge (and by implication stress) can be varied at will, providing a tool to control the Si/insulator interface. The bottom layer displays good electrical characteristics and the structure is resistant to boron penetration. In this work CVD oxynitride has been used as a membrane to do a controlled diffusion of O_2 and oxidation of Si at relatively high temperatures. In principle, it is possible to replace this CVD oxynitride layer by other oxynitrides or other dielectrics.

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